Abstract

Field-effect transistor with local source/drain insulation and associated fabrication method

The invention relates to a field-effect transistor with local source/drain insulation and to an associated fabrication method, a source depression (SV) and a drain depression (DV) being formed in a manner spaced apart from one another in a semiconductor substrate (1) and a depression insulation layer (VI) being formed at least in a bottom region of the source and drain depressions (SV, DV) and an electrically conductive filling layer (F), for realizing source and drain regions (S, D), filling the source and drain depressions (SV, DV). Together with a gate dielectric (3) and a gate layer (4), a field-effect transistor with reduced junction capacitances is obtained in this way.

Figure 1